Claims:

1. A circuit to encode binary digital signals so as to reduce EMI emissions during signal transmission across a bus or interconnect comprising:

circuitry to generate a pseudo-random pattern of binary digital signals; and

circuitry to apply logic operations to selected binary digital signals, the selected binary digital signals to be encoded prior to signal transmission across the bus or interconnect, with selected binary digital signals of the pseudo-random pattern in order to reduce the harmonic content of the selected binary digital signals to be encoded.

2. The circuit of claim 1, wherein the logic operations comprise one of a logical exclusive OR operation and a logical exclusive NOR operation.

3. The circuit of claim 2, wherein the binary digital signals comprise regular binary digital signals.

4. The circuit of claim 3, wherein the regular binary digital signals comprise video digital interface signals.

5. The circuit of claim 3, wherein the regular binary digital signals comprise digital clock signals.

6. The circuit of claim 1, wherein the circuitry to generate a pseudo-random pattern of binary digital signals comprises more than one pseudo-random pattern generator to generate more than one pseudo-random pattern; and wherein the circuitry to apply logic operations comprises circuitry to apply logic operations to selected binary digital signals, the selected binary digital signals to be encoded prior to signal transmission across the bus or interconnect, with selected binary digital signals of the pseudo-random patterns in order to reduce the harmonic content of the selected binary digital signals to be encoded.

7. The circuit of claim 1, wherein said circuit is embodied on a motherboard.

8. The circuit of claim 1, wherein said motherboard is embodied in a personal computer.

9. A method of encoding binary digital signals so as to reduce EMI emissions during signal transmission across a bus or interconnect comprising:

generating a pseudo-random pattern of binary digital signals;

applying logic operations to selected binary digital signals, the selected binary digital signals to be encoded prior to signal transmission across the bus or interconnect, with selected binary digital signals of the pseudo-random pattern in order to reduce the harmonic content of the selected binary digital signals to be encoded.

10. The method of claim 9, wherein the logic operations comprise one of a logical exclusive OR operation and a logical exclusive NOR operation.

11. The method of claim 9, wherein the binary digital signals comprise regular binary digital signals.

12. The method of claim 11, wherein the regular binary digital signals comprise video digital interface signals.

13. The method of claim 11, wherein the regular binary digital signals comprise digital clock signals.

14. The method of claim 9, wherein generating a pseudo-random pattern of binary digital signals comprises generating more than one pseudo-random pattern; and wherein applying logic operations comprises applying logic operations to selected binary digital signals, the selected binary digital signals to be encoded prior to signal transmission across the bus or interconnect, with selected binary digital signals of the pseudo-random patterns in order to reduce the harmonic content of the selected binary digital signals to be encoded.

15. A circuit to decode binary digital signals that have been encoded so as to reduce EMI emissions during signal transmission across a bus or interconnect comprising:

circuitry to apply logic operations to selected encoded binary digital signals to be decoded,

the encoded binary digital signals being encoded to reduce the harmonic content of the pre-encoded binary digital signals, with selected binary digital signals of a pseudo-random pattern used to encode the encoded binary digital signals.

16. The circuit of claim 15, wherein the logic operations comprise one of a logical exclusive OR operation and a logical exclusive NOR operation.

20. The circuit of claim 15, wherein the circuitry to apply logic operations includes circuitry to generate a pseudo-random pattern of binary digital signals.

21. The circuit of claim 20, wherein the circuitry to generate a pseudo-random pattern of binary digital signals comprises more than one pseudo-random pattern generator to generate more than one pseudo-random pattern; and wherein the circuitry to apply logic operations comprises circuitry to apply logic operations to selected binary digital signals, the selected binary digital signals to be encoded prior to signal transmission across the bus or interconnect, with selected binary digital signals of the pseudo-random patterns in order to reduce the harmonic content of the selected binary digital signals to be encoded.

22. The circuit of claim 15, wherein said circuit is embodied on a motherboard.

23. The circuit of claim 15, wherein said motherboard is embodied in a personal computer.

24. A method of decoding binary digital signals that have been encoded so as to reduce EMI emissions during signal transmission across a bus or interconnect comprising:

applying logic operations to selected encoded binary digital signals to be decoded, the encoded binary digital signals being encoded to reduce the harmonic content of the pre-encoded binary digital signals, with selected binary digital signals of a pseudo-random pattern used to encode the encoded binary digital signals.

25. The method of claim 24, wherein the logic operations comprise one of a logical exclusive OR operation and a logical exclusive NOR operation.

26. The method of claim 24, and further comprising, generating a pseudo-random pattern of binary digital signals.

27. The method of claim 26, wherein generating a pseudo-random pattern of binary digital signals comprises generating more than one pseudo-random pattern of binary digital signals; and wherein applying logic operations comprises applying logic operations to selected binary digital signals, the selected binary digital signals to be encoded prior to signal transmission across the bus or interconnect, with selected binary digital signals of the pseudo-random patterns in order to reduce the harmonic content of the selected binary digital signals to be encoded.

28. A circuit to encode binary digital signals so as to reduce EMI emissions during signal transmission across a bus or interconnect comprising:

circuitry to apply at least one pseudo-random pattern of binary digital signals to encode selected binary digital signals so as to reduce the harmonic content of the selected binary digital signals.

29. The circuit of claim 28, wherein the binary digital signals to be encoded comprise regular binary digital signals.

30. The circuit of claim 29, wherein the regular binary digital signals comprise video digital interface signals.

31. The circuit of claim 29, wherein the regular binary digital signals comprise digital clock signals.

32. The circuit of claim 28, wherein said circuit is embodied on a motherboard.

33. The circuit of claim 28, wherein said motherboard is embodied in a personal computer.

34. A method of encoding binary digital signals so as to reduce EMI emissions during signal transmission across a bus or interconnect comprising:

applying at least one pseudo-random pattern of binary digital signals to encode selected binary digital signals so as to reduce the harmonic content of the selected binary digital signals.

35. The method of claim 34, wherein the binary digital signals comprise regular binary digital signals.

36. The method of claim 35, wherein the regular binary digital signals comprise video digital

interface signals.

34 ~~37~~. The method of claim ~~35~~ 32, wherein the regular binary digital signals comprise digital clock signals.

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